



Fine grinding of silicon wafers: a mathematical model for grinding marks

S. Chidambaram^a, Z.J. Pei^{a,*}, S. Kassir^b

^a Department of Industrial and Manufacturing Systems Engineering, Kansas State University, 237 Durland Hall, Manhattan, KS 66506-5101, USA

^b Strasbaugh, Inc., 825 Buckley Road, San Luis Obispo, CA 93401, USA

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Abstract

The majority of today's integrated circuits are constructed on silicon wafers. Fine-grinding process has great potential to improve wafer quality at a low cost. Three papers on fine grinding were previously published in this journal [Microchip Fabrication, McGraw-Hill, New York, 2000; Silicon Machining Symposium, American Society For Precision Engineering, St. Louis, Missouri, April, 1998; East Bay Business Times, February 12, 2002]. The first paper discussed its uniqueness and special requirements. The second one presented the results of a designed experimental investigation. The third paper developed a mathematical model for the chuck shape, addressing one of the technical barriers that have hindered the widespread application of this technology: difficulty and uncertainty in chuck preparation. As a follow up, this paper addresses another technical barrier: lack of understanding on grinding marks. A mathematical model to predict the locus of the grinding lines and the distance between two adjacent grinding lines is first developed. With the developed model, the relationships between grinding marks and various process parameters (wheel rotational speed, chuck rotational speed, and wheel diameter) are then discussed. Finally, results of pilot experiments to verify the model are discussed.

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1. Introduction

1.1. Silicon wafers and their manufacturing processes

Integrated circuits (ICs) are built on semiconductor wafers. Over 90% of semiconductor wafers are silicon [1]. About 150 million silicon wafers of different sizes are manufactured each year worldwide [2]. In 2000, the worldwide revenue generated by silicon wafers was \$ 7.5 billion [3]. Semiconductor devices built on these wafers generated \$ 200 billion in revenues [4].

Manufacturing of silicon wafers starts with growth of silicon ingots. A sequence of processes is needed to turn an ingot into wafers. As shown in Fig. 1, this typically consists of the following processes [5–8]:

1. slicing, to slice a silicon ingot into wafers of thin disk shape;
2. edge profiling or chamfering, to chamfer the peripheral edge portion of the wafer;
3. flattening (lapping or grinding), to achieve a high degree of parallelism and flatness of the wafer;
4. etching, to chemically remove the damage induced by slicing and flattening without introducing further mechanical damage;
5. rough polishing, to obtain a mirror surface on the wafer;
6. fine polishing, to obtain final mirror surface; and
7. cleaning, to remove the polishing agent or dust particles from the wafer surface.

1.2. Wafer flatness

As the starting materials for fabrication of most ICs, silicon wafers must be very flat in order to print circuits on them by lithographic processes. Wafer flatness

* Corresponding author. Tel.: +1-785-532-3436; fax: +1-785-532-3738.

E-mail address: zpei@ksu.edu (Z.J. Pei).

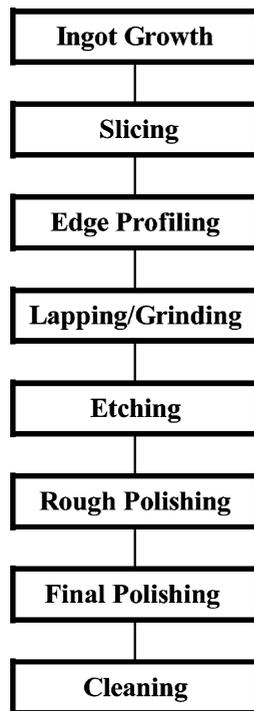


Fig. 1. Traditional process flow for manufacturing of silicon wafers.

directly impacts device line-width capability, process latitude, yield, and throughput [9,10]. Continuing reduction in feature sizes demands increasingly flatter wafers [11].

Wafer flatness can be characterized in terms of a global or site parameter. A frequently used parameter to measure site flatness is SBIR (site flatness, back reference surface, ideal reference plane, range) [12]. It is the sum of the maximum positive and negative deviations of the surface in a certain area of the wafer from a theoretical reference plane that is approximately parallel to the back surface of the wafer and intersects the front surface at the center of the area. Typical size of the area is $20 \times 20 \text{ mm}^2$ for ordinary wafers and $30 \times 35 \text{ mm}^2$ for advanced applications.

For wafers manufactured by a traditional process flow, only a small percentage meet tight flatness specifications. The wafers that do not meet the specifications are often rejected, causing high yield-loss. Silicon wafer manufacturers are under tremendous pressure to develop alternative process flows or new processes to produce flatter wafers at an affordable cost.

1.3. Approaches to flatness improvement

Several approaches have been proposed to improve flatness. The first approach is double-side polishing [6,13]. If operating properly, it is capable of achieving superior flatness. It has become the standard polishing operation for 300 mm wafers. However, its application to wafers with diameter of 200 mm and less has stalled.

The primary reason is that double-side polishing creates mirror finish surfaces on both front side and backside of the wafer. This causes problems in IC fabs. Respective sensors of processing equipment cannot distinguish the front side from the backside. Furthermore, wafers with both sides mirror polished tend to slip out during handling process [6].

The second approach is called PACE, plasma-assistant chemical etching [9]. The PACE operation requires point-by-point thickness profile data that typically cover several thousand discrete positions on the front surface of the wafer. The PACE machine removes the material at each position on the wafer according to the profile data. Excellent flatness has been reported with PACE. The major drawbacks of this approach are high capital investment and low throughput.

Another approach is etched-wafer fine grinding [14]. Fine grinding is used to partially replace the rough-polishing process, addressing two problems associated with the traditional process flow: poor flatness and high cost.

Fine grinding of etched wafers first appeared in public domain through the US patent by Vandamme et al. [14]. Pei and Strasbaugh [15] reported an experimental study on the effects of grinding wheels, process parameters, and coolant. They also presented results of a designed experiment [16] in which three-factor, two-level full factorial design was used to reveal the main and interaction effects of three process parameters (wheel speed, chuck speed, and feedrate) on process outputs (grinding force, spindle motor current, cycle time, surface roughness, and grinding marks). Chidambaram et al. [17] developed a mathematical model to predict the relations between the chuck shape and the setup parameters, aiming to overcome one of the technical barriers that have hindered the widespread application of fine grinding: difficulty and uncertainty of chuck preparation. Oh et al. [18] reported a study on damage induced by fine grinding.

1.4. Benefits of fine grinding

Generally, a wet etching process can negatively affect flatness [19], and extended polishing (of single-side, wax-mounting type) can deteriorate flatness [14]. Because fine grinding will improve the flatness of etched wafers and reduce the removal amount of rough polishing by 25–50%, the flatness of polished wafers can be improved. Furthermore, fine grinding can reduce manufacturing costs due to the following reasons: (1) it reduces polishing removal amount and cuts down the time of the expensive polishing operation, (2) it improves flatness and lowers the yield-loss, and (3) it grinds wafers to a uniform thickness and eliminates the sorting operation for production lines that polish multiple wafers simultaneously. If multiple wafers with different thickness are mounted on the same polishing plate, these wafers will not have good flatness after pol-

ishing. Without fine grinding, the thickness variation among etched wafers is quite large; hence, a sorting operation is often needed, adding extra cost.

Introducing fine-grinding step requires capital investment (purchasing and installation of grinder) and additional costs (utilities, consumables, and labor). Furthermore, a cleaning step is usually required after fine grinding (before polishing). Adoption of fine grinding into a production line makes economic sense only if the cost reduction is greater than the added cost. As illustrated in Fig. 2, the economic benefit of fine grinding will become more prominent when the flatness specification becomes tighter (say, $SBIR < S_c$).

Although fine grinding has been implemented in some production lines with good results, it cannot be economically justified for many other lines. To gain widespread application, the cost curve with fine grinding in Fig. 2 has to be much lower. This cost curve can be lowered by further reducing the polishing amount, because the smaller the polishing amount, the shorter the polishing time and the less expensive the polishing step. Furthermore, the smaller the polishing amount, the less the degradation of flatness and the lower the yield-loss. However, further reduction of polishing amount becomes very difficult due to the lack of fundamental understanding about some issues in fine grinding. One such issue is the grinding marks left on the wafer surface after fine grinding.

1.5. Grinding marks

Fig. 3 shows pictures of two silicon wafers after fine grinding and polishing. Wafer B is good since no patterns are visible, but wafer A is not acceptable due to visible grinding marks. One approach to correct wafer A is to keep polishing it until all grinding marks are gone. This will lengthen the polishing time, increase manufacturing costs, and deteriorate flatness. A better approach is to optimize the fine-grinding process so that grinding marks can be removed with minimum polishing. The success of the latter approach depends on whether or not the following questions can be answered:

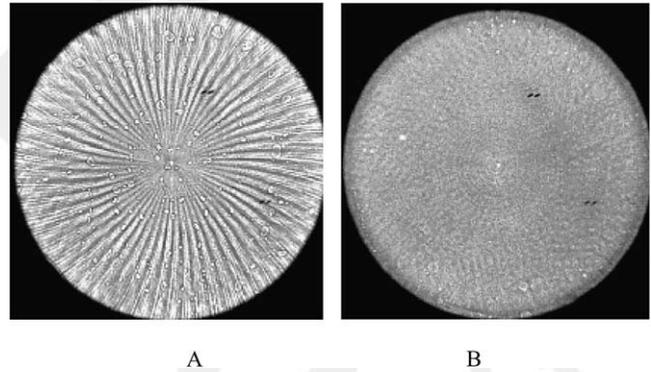


Fig. 3. Comparison of wafers with and without grinding marks.

How are grinding marks generated? How do grinding parameters affect grinding marks? How can grinding marks be controlled? What kinds of grinding marks are easier for polishing process to remove?

Pei and Strasbaugh [20] have previously reported a preliminary investigation into grinding marks. That investigation covers (a) nature of grinding marks, (b) factors that have effects on grinding marks, and (c) approaches to reduce grinding marks. Further research is needed to answer those questions presented in the preceding paragraph.

1.6. Outline of this paper

The future of fine grinding is largely determined by whether or not the polishing amount can be further reduced. However, the polishing amount has to be large enough to remove all grinding marks. This paper will present a mathematical model on grinding marks. The objectives are to understand the formation mechanisms of grinding marks and to provide guidance to optimize the grinding process for the minimum polishing amount.

This paper is organized into five sections. Following this introduction section, Section 2 develops the mathematical model. In Section 3, the model is used to predict the relations between the grinding marks (the locus of grinding lines and the distance between adjacent lines) and the grinding parameters. Section 4 discusses the pilot experiments performed to verify the model. Conclusions are drawn up in Section 5.

2. Development of mathematical model

The literature most relevant to grinding marks includes analyses on vertical-spindle surface grinding using conventional wheels [21], diamond cup wheel grinding of parabolic and toroidal surface on ceramics for mirrors [22,23], and precision cylindrical face grinding using a narrow ring superabrasive wheel [24]. These analyses are instrumental to the model development for wafer grinding, but cannot be applied directly.

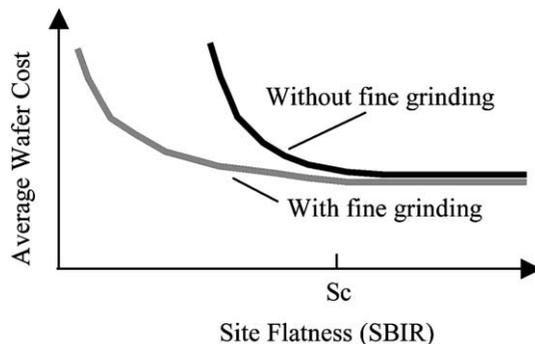


Fig. 2. Effects of flatness specification on wafer cost.

Fig. 4 illustrates the wafer grinding process. The grinding wheel shown is a diamond cup wheel. The wafer is held on the porous ceramic chuck by means of vacuum. The axis of rotation for the grinding wheel is offset by the distance of the wheel radius relative to the axis of rotation for the wafer. During grinding, the grinding wheel and the wafer rotate about their own axes of rotation simultaneously, and the wheel is fed towards the wafer along its axis of rotation.

Development of the model in this paper is based on the assumption that the grinding wheel behaves like a single-point tool. This assumption has been validated by the authors' previous research [7,20] and also used by other researchers [24]. The grinding wheel removes the work material from the edge to the center along the arch MO, as shown in Fig. 5. Two coordinate systems XOY and UO₁V, are used to define all the points on the wafer and the grinding wheel. The origin of the UO₁V coordinate system is at the center of the grinding wheel and the origin of the XOY coordinate system is at the center of the wafer. The UO₁V system is offset from the XOY system along the Y-axis by a distance of R, the radius of the grinding wheel. The grinding wheel revolves about its center O₁ at a speed of N_s (rpm, or revolution per minute). The wafer revolves about its center O at a speed of N_c (rpm). The radius of the wafer is R_w.

For any point P with coordinates (u, v) in the UO₁V system and (x, y) in the XOY system, there is the following relation.

$$\begin{bmatrix} x \\ y \\ 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & -R \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} u \\ v \\ 1 \end{bmatrix} \quad (1)$$

The movement of the single cutting point while in contact with the wafer will generate the arc MO if the

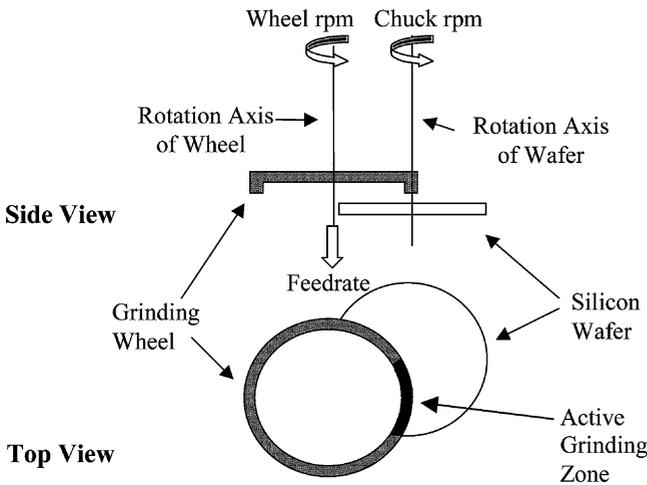


Fig. 4. Illustration of wafer grinding.

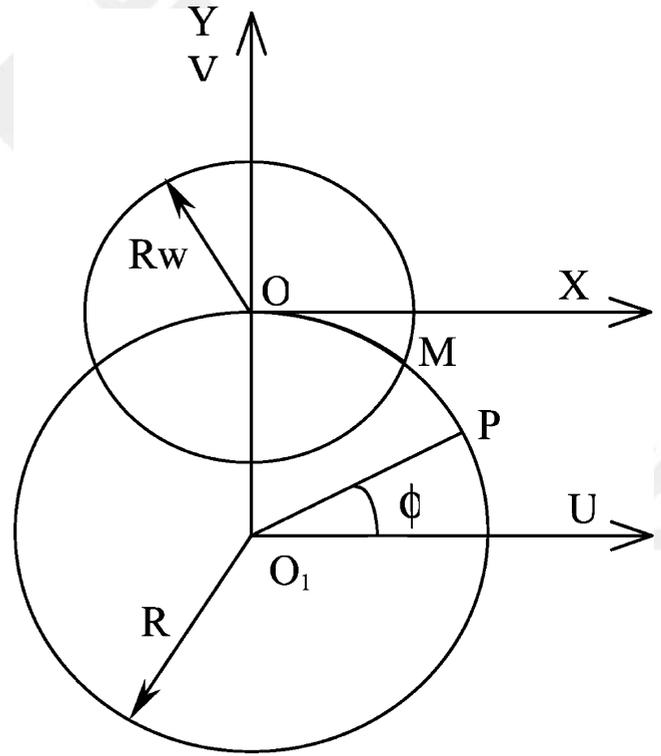


Fig. 5. Illustration of coordinate systems.

wafer is stationary. The arc can be described by the following equations in the UO₁V system.

$$\begin{aligned} u &= R \cdot \cos\phi = R \cdot \cos(2\pi \cdot N_s \cdot t) \\ v &= R \cdot \sin\phi = R \cdot \sin(2\pi \cdot N_s \cdot t) \end{aligned} \quad t_1 \leq t \leq \frac{1}{4N_s} \quad (2)$$

where, ϕ is the angle between the line OP and the U-axis, and t_1 is the time it takes for point P to move from coordinate (R, 0) to point M along the circle with center at O₁ and radius of R. The following equation can be used to calculate t_1 .

$$t_1 = \frac{1}{2\pi N_s} \left(\frac{\pi}{2} - 2\arcsin\left(\frac{R_w}{2R}\right) \right) \quad (3)$$

Through Eq. (1), arch MO can be described in the XOY coordinate system by the following equations.

$$\begin{aligned} x &= u = R \cdot \cos(2\pi \cdot N_s \cdot t) \\ y &= v - R = R \cdot \sin(2\pi \cdot N_s \cdot t) - R \end{aligned} \quad t_1 \leq t \leq \frac{1}{4N_s} \quad (4)$$

Let point M at the edge of the wafer be the starting point of the first grinding line. The coordinates of point M can be calculated from Eq. (4) if letting $t = t_1$. The starting points of subsequent grinding lines can be obtained from Eq. (4) when $t = t_n$ where t_n is given by the following equation.

$$t_n = \frac{1}{2\pi N_s} \left(\frac{\pi}{2} - 2\arcsin\left(\frac{R_w}{2R}\right) \right) + \frac{n-1}{N_s} \quad n = 2, 3, 4, \dots \quad (5)$$

Note that the arch MO described by Eqs. (2) or (4) is

the locus of a grinding line if the wafer keeps stationary. Due to the simultaneous revolution of the wafer, point P will be offset to P' on the wafer as shown in Fig. 6. In order to get the coordinates of point P' , the following parameters are necessary.

$$\theta_0 = \arctan\left(\frac{y}{x}\right) \quad (6)$$

$$\Delta\theta = 2\pi \cdot N_c \cdot (t - t_1) \quad (7)$$

$$\theta = \theta_0 - \Delta\theta \quad (8)$$

$$r = \sqrt{x^2 + y^2} \quad (9)$$

Thus, the coordinates of P' can be written as (x', y') .

$$x' = r \cdot \cos(\theta) \quad (10)$$

$$y' = r \cdot \sin(\theta)$$

The above mathematical equations are used to develop a program using a commercial software package Matlab (The MathWorks, Inc., 3 Apple Hill Drive, Natick, MA 01760, USA). This program will accept grinding parameters as input variables and plot the grinding marks as output. It will also calculate the distance between adjacent grinding lines.

3. The effects of process parameters on grinding marks

In the preceding section, a mathematical model has been developed to predict the grinding marks when the process parameters (i.e., wheel rotational speed, chuck rotational speed, and wheel radius) are known. Next, this model will be used to investigate the effects of process parameters on grinding marks.

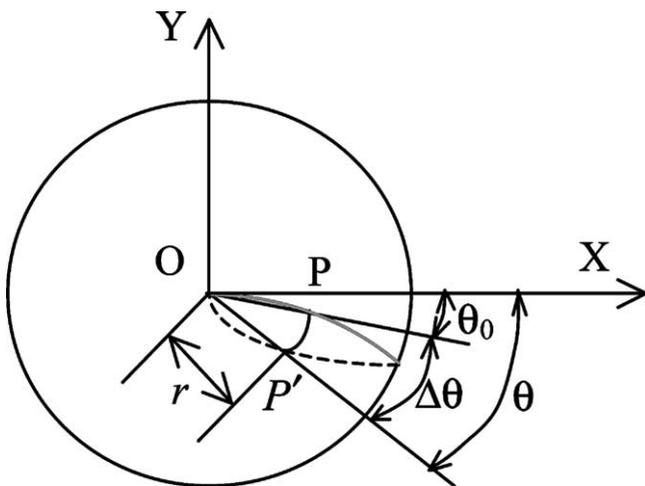


Fig. 6. Offset of point P to P' due to wafer rotation.

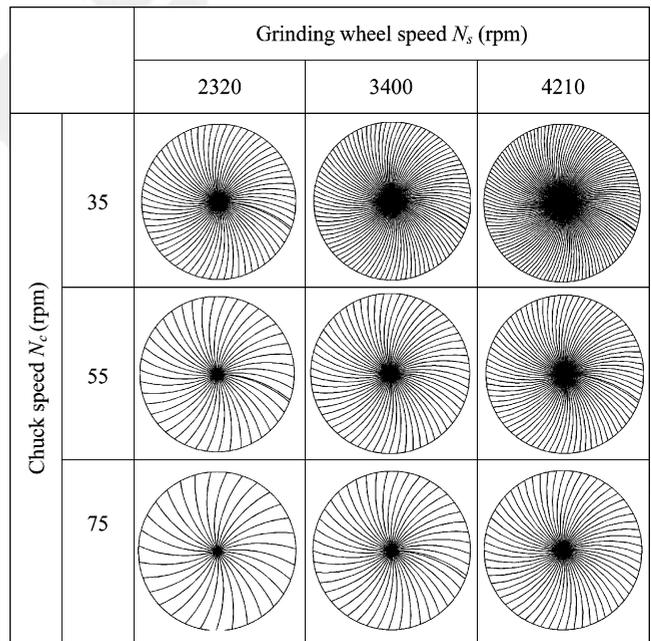


Fig. 7. Effects of wheel speed and chuck speed on grinding marks.

3.1. Effects on the distance between adjacent grinding lines

Fig. 7 shows the variation of the distance between adjacent grinding lines as wheel rotational speed and chuck speed change. It can be seen that, as chuck speed increases, the distance between adjacent grinding lines increases. Furthermore, as wheel speed increases, the line distance decreases. The above observation can also be made from Fig. 8.

Fig. 9 shows the influence of the N_c/N_s ratio on the line distance. N_c is the chuck speed and N_s the wheel speed. An important finding is that the line distance is determined by the N_c/N_s ratio. As the speed ratio increases, the line distance increases.

Fig. 10 shows the effects of wheel radius. It is obvious that the wheel radius has no effects on the line distance.

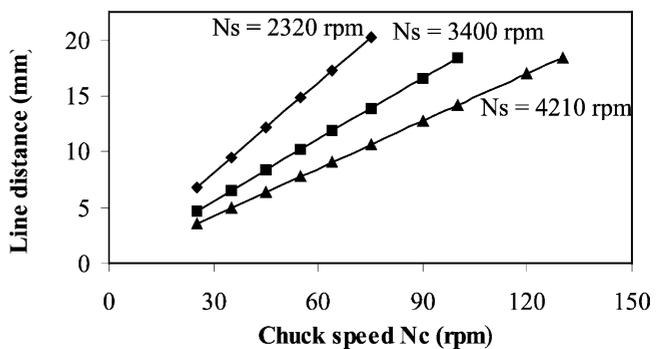


Fig. 8. Effect of wheel speed and chuck speed on line distance of grinding marks.

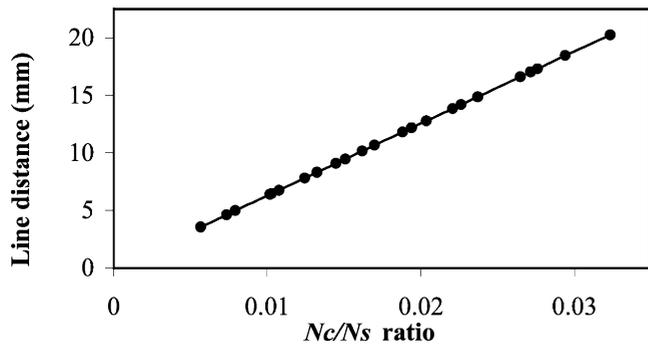


Fig. 9. Effect of speed ratio on line distance of grinding marks.

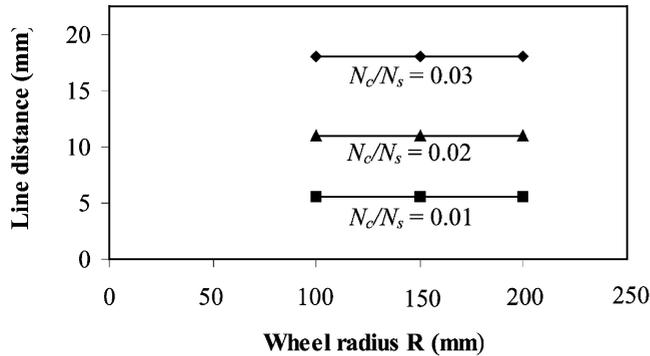


Fig. 10. Effect of grinding wheel radius on line distance of grinding marks.

3.2. Effects on the curvature of grinding lines

Fig. 11 shows the variation of a grinding line as wheel radius and N_c/N_s ratio change. Negative speed ratio

		Wheel radius R (mm)		
		100	140	175
N _c /N _s ratio	-0.25			
	-0.05			
	0.05			
	0.25			

Fig. 11. Effects of wheel radius and speed ratio on the curvature of grinding marks.

means that the chuck rotates in the reversed direction. It can be seen that the grinding line tends to be less curved as the N_c/N_s ratio increases, or as the wheel radius increases.

4. Pilot experimental verification

4.1. Experimental conditions and procedures

Grinding experiments are conducted on a Strasbaugh Model 7AF wafer grinder (Strasbaugh, Inc., San Luis Obispo, California). The grinding wheel used is a diamond cup wheel. The grit size is mesh no. 320 for the coarse grinding wheel and mesh no. 2000 for the fine-grinding wheel. The radius of the wheels is 140 mm. Single crystal silicon wafers of 200 mm in diameter with (1 0 0) plane as the major surface (the front or back surface of the wafer) are used for this investigation. Unless otherwise stated, the feedrate is 1.2 $\mu\text{m/s}$, and the grit size of the wheel is mesh no. 320.

During grinding, deionized (purified) water is used to cool the grinding wheel and the wafer surface. For this study, coolant is provided to the inner side of the cup wheel. The coolant flow rate is 3.2 gal/min.

To obtain the distance between two successive grinding lines, the number of distinctive grinding lines on the wafer is counted. Dividing the circumference of the wafer by the number of grinding lines gives the line distance.

Selected ground wafers are further polished for magic mirror inspection. The purpose of this polishing operation is to provide a shining surface for the magic mirror inspection. Polishing experiments are conducted on a Strasbaugh Model 6DZ wax mount polisher (Strasbaugh, Inc., San Luis Obispo, California). The polishing slurry used is Rodel 1540, and the polishing pad used is Suba 500, both are manufactured by Rodel (Phoenix, Arizona). More information on the slurry and pad can be found at: <http://www.rodel.com>. The polished wafers are then inspected under a magic mirror (Model YIS-200SP-4, HOLOGENiX, Huntington Beach, California). More information on the magic mirror technology can be found in [25–27].

4.2. Experimental results

Figs. 12 and 13 show the comparison of experimental and predicted effects on the line distance of grinding marks. It can be seen that the experimental results matched very well with the predicted values.

Fig. 14 shows the comparison of a magic mirror picture of a ground wafer and the predicted pattern of grinding marks. It can be seen that both the line distance and curvature of the predicted grinding marks match well with the magic mirror picture.

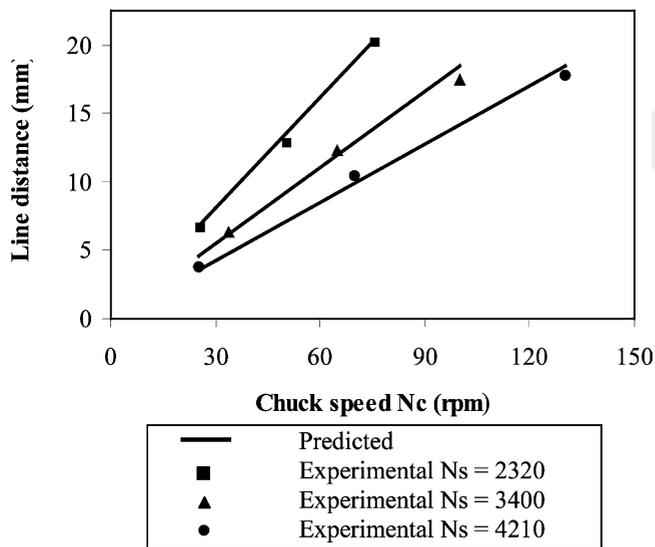


Fig. 12. Comparison of experimental and predicted effects of wheel speed and chuck speed.

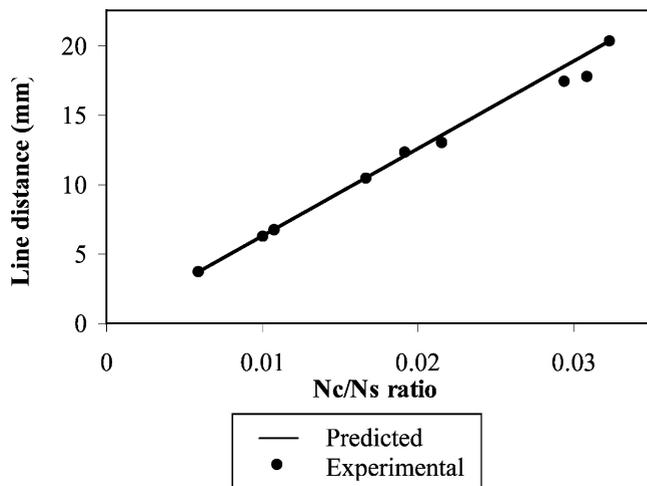


Fig. 13. Comparison of experimental and predicted effects of speed ratio.

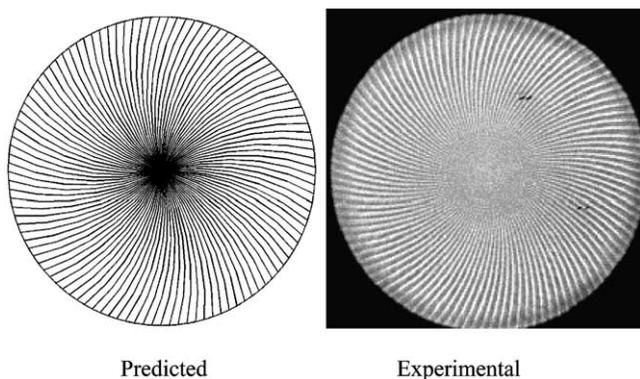


Fig. 14. Comparison of experimental and predicted grinding marks. ($N_c=40$ rpm, $N_s=4350$ rpm, feedrate= $0.1 \mu\text{m s}^{-1}$, grit size=#2000)

5. Conclusions

A mathematical model is developed to predict the line distance and locus of grinding marks in wafer grinding. The model predicts the following relations between the grinding marks and process parameters:

1. The distance between the adjacent grinding lines is determined by the ratio of chuck speed and wheel speed. As the speed ratio increases, the line distance increases.
2. The speed ratio also affects the curvature of the grinding lines. As the speed ratio increases, the grinding lines tend to become less curved.
3. As the radius of the grinding wheel increases, the grinding lines tend to become less curved.

The results of pilot experiments agree well with the model predictions.

The mathematical model developed may seem simple or even trivial. However, the relationship between grinding parameters and grinding marks has not been available in literature. This model provides a powerful tool to optimize grinding processes so that grinding marks can be easily removed by subsequent polishing processes. Polishing can effectively remove high-frequency surface roughness (caused by individual diamond grains in the grinding wheel), but its ability to remove grinding marks heavily depends on their frequency (or wavelength). With this mathematical model, frequency and curvature of grinding marks can be controlled by selecting proper grinding parameters. This, in turn, makes it possible to systematically study grinding and polishing processes to eliminate grinding marks.

Validation of this mathematical model has further substantiated the assumption that the grinding wheel behaves like a single-point cutter (due to dynamic unbalance). This suggests that any measures to reduce the unbalance of the grinding wheel should help reduce grinding marks.

The mathematical model developed in this paper is also applicable to other wafer grinding applications. Two examples are grinding of wire-sawn wafers and grinding of backsides of completed IC wafers.

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